

# Documents Useful for Understanding Elcor

## **Acyclic scheduling**

Inter-region scheduling [1].

## **Modulo scheduling**

Modulo scheduling of DO-loops [2].

Register-pressure sensitive modulo scheduling [3].

## **Register allocation**

Rotating register allocation [4].

## **If-conversion and the use of predicates**

If-conversion to form predicated code [5].

## **Analysis of predicated code**

Analysis of predicated code [6].

## **Critical path reduction (CPR)**

Compiler transformations to reduce the length of the critical path through a computation [7, 8].

## **Machine description**

The machine description database and query interface used by the ILP compiler to understand the relevant details of the target processor [9, 10].

# Bibliography

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4. B. R. Rau, M. Lee, P. Tirumalai and M. S. Schlansker. Register Allocation for Software Pipelined Loops. Proc. SIGPLAN'92 Conference on Programming Language Design and Implementation (San Francisco, June 17-19 1992).
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10. S. Aditya, V. Kathail and B. R. Rau. Elcor's Machine Description System: Version 3.0. HPL Technical Report HPL-98-128. Hewlett-Packard Laboratories, July 1998.